

TIMING GENERATOR OF FLAT PANEL DISPLAY AND POLARITY ARRANGEMENT CONTROL SIGNAL GENERATION METHOD THEREFOR

BACKGROUND OF THE INVENTION

5 1. Field of the Invention

The present invention relates to flat panel displays and, more particularly, to a timing generator of flat panel display and polarity arrangement control signal generation method therefor.

2. Description of Related Art

10 Flat panel display is the dominant type of display in the market. Currently, there are three widely used flat panel displays, namely liquid crystal displays (LCDs), thin film transistor LCDs (TFT-LCDs), and organic electroluminescence display (OLEDs). The principles of LCDs or TFT-LCDs are that the orientation of liquid crystal molecules is controlled
15 by bias and in turn the light transmission thereof can be controlled for generating gray scales with a color effect.

However, the liquid crystal molecules may be permanently deformed, resulting in a poor display quality if the liquid crystal molecules are continuously biased by a voltage having the same polarity. Currently, there
20 are a couple of voltage polarity inverting control methods as detailed below. In FIG. 1, a display panel 100 is divided into a plurality of blocks in which a pixel 111 of a first block 110 (i.e., area A) has a polarity opposite to that of a corresponding pixel 121 of an adjacent second block (i.e., area B) or opposite to that of a corresponding pixel 131 of an adjacent third block (i.e.,

area C). But, the polarities of the pixel 111 of the first block 110 and the corresponding pixel of a fourth block (i.e., area D) are the same.

This is a block-based configuration (e.g., blocks 110, 120, 130, and 140). In a case of column signals of the display panel 100 driven by time division multiplexing, an input pattern can cause a sum of all effective voltages of one polarity applied to the liquid crystal to be much larger than a sum of all effective voltages of the opposite polarity applied to the liquid crystal, which may cause cross-talk. As a result, the display quality will be lowered because picture of one block of the display panel 100 may adversely affect brightness of the pictures of adjacent blocks thereof.

In FIG. 2, a configuration of irregularly changing the polarity arrangement of a panel 200 in the vertical direction (i.e., data line direction) is shown in which any two adjacent blocks have opposite polarities. It is seen that positive and negative polarities along any row line are alternate. However, the above problem still exists. In detail, in a case of column signals of the panel 200 driven by time division multiplexing, an input pattern can cause a sum of all effective voltages of one polarity applied to the liquid crystal to be much larger than a sum of all effective voltages of the opposite polarity applied to the liquid crystal. It may cause cross-talk. As a result, the display quality will be lowered. Thus, the need for improvement still exists in order to mitigate and/or obviate the aforementioned problems.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a timing generator of

flat panel display and polarity arrangement control signal generation method therefor so as to decrease cross-talk and improve display quality.

In one aspect of the present invention there is provided a timing generator of a panel display for generating a PAC (Polarity Arrangement Control) signal and sending the same to a data driver so that the data driver is operative to control a polarity of display data based on the PAC signal and send the display data to a display panel, the timing generator comprising a storage unit for storing a plurality of sets of polarity data and a plurality of PAC signals wherein each set of polarity data includes a plurality of data polarities and each set of polarity data corresponds to one of the PAC signals; an operation unit for receiving the display data, the plurality of sets of polarity data, and a corresponding one of the PAC signals so that the operation unit is operative to perform an inner product operation with respect to the polarity data of each set of polarity data and the display data for obtaining a sum of a plurality of coupling voltages corresponding to the polarity data of each set of polarity data; and a comparison unit for comparing the sum of coupling voltages with a predetermined value, and outputting the PAC signal if the sum of coupling voltages is smaller than the predetermined value.

In another aspect of the present invention there is provided a timing generator of a panel display for generating a PAC signal and sending the same to a data driver so that the data driver is operative to control a polarity of display data based on the PAC signal and send the display data to a display panel, the timing generator comprising a storage unit for storing a

plurality of sets of polarity data and a plurality of PAC signals wherein each set of polarity data includes a plurality of data polarities and each set of polarity data corresponds to one of the PAC signals; an operation unit for receiving the display data, the plurality of sets of polarity data, and a
5 corresponding one of the PAC signals so that the operation unit is operative to perform an inner product operation with respect to each set of polarity data and the display data for obtaining a sum of a plurality of coupling voltages corresponding to the polarity data; and a comparison unit for comparing the sums of coupling voltages each other for selecting a smallest
10 sum of coupling voltages, and outputting a corresponding one of the PAC signals to the data driver.

In still another aspect of the present invention there is provided a method of generating PAC signal, comprising the steps of receiving display data, at least one set of predetermined polarity data, and at least one PAC
15 signal corresponding to the at least one set of PAC data; performing an inner product operation with respect to the at least one set of PAC data and the display data for obtaining a sum of at least one coupling voltage; comparing the sum of at least one coupling voltage with a predetermined value; and outputting the PAC signal of polarity data corresponding to the sum of at
20 least one coupling voltage if the sum of at least one coupling voltage is smaller than the predetermined value.

In a further aspect of the present invention there is provided a method of generating PAC signal, comprising the steps of receiving display data, at least one set of predetermined polarity data, and at least one PAC signal

corresponding to the at least one set of PAC data; performing an inner product operation with respect to each set of polarity data and the display data for obtaining a sum of a plurality of coupling voltages corresponding to the at least one set of polarity data; comparing the sums of coupling
5 voltages each other for selecting a smallest sum of coupling voltages; and outputting a corresponding PAC signal having the smallest sum of coupling voltages.

Other objects, advantages, and novel features of the invention will become more apparent from the detailed description when taken in
10 conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically depicts a conventional voltage polarity inverting control method by dividing a display panel into a plurality of blocks;

FIG. 2 schematically depicts another conventional configuration having
15 alternate positive and negative polarities along any row line of a display panel;

FIG. 3 schematically depicts a structure applicable to the invention;

FIG. 4 is a block diagram according to a first preferred embodiment of the invention;

20 FIG. 5 is a flow chart of the first preferred embodiment of the invention;

FIG. 6 illustrates operating voltage versus grey level and polarity for the first preferred embodiment of the invention;

FIG. 7 is a block diagram according to a second preferred embodiment of the invention; and

FIG. 8 is a flow chart of the second preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

With reference to FIG. 3, there is shown a structure constructed in accordance with the invention comprising a display panel 300, a scan driver 310, a timing generator 320, and a data driver 330. Each component will be described in detail below. The display panel 300 comprises a plurality of pixels 301. A plurality of scan lines 340 are interconnected the scan driver 310 and the pixels 301 of the display panel 300. Likewise, a plurality of data lines 350 are interconnected the data driver 330 and the pixels 301 of the display panel 300. In the embodiment, preferably, the display panel 300 is an LCD panel. The timing generator 320 is adapted to generate optimum PAC (polarity arrangement control) signals and send the same to the data driver 330. Each PAC signal corresponds to one of a plurality of data polarities. As such, the data driver 330 is able to select one of a plurality of sets of predetermined polarity data based on the PAC signal. Thus, the polarities of the pixels 301 of the display panel 300 can be controlled. As a result, it is possible of decreasing cross-talk and improving display quality. As to how the timing generator 320 generates optimum PAC signals will be described in detail below.

With reference to FIG. 4, the timing generator 320 according to a first preferred embodiment of the invention comprises a storage unit 3211, an operation unit 3212, a comparison unit 3213, and a counting unit 3214. Preferably, the operation unit 3212 is comprised of an adder and a control

circuit in the embodiment. Preferably, the storage unit 3211 is implemented as a random access memory (RAM) for storing the plurality of sets of polarity data and the plurality of PAC signals. Further, each set of polarity data comprises a plurality of data polarities. Furthermore, each set of polarity data corresponds to one PAC signal. Preferably, there are 16 sets of polarity data and there are 300 data polarities in the embodiment.

A flow chart of the first preferred embodiment of the invention will be illustrated in FIG. 5 in conjunction with FIG. 6. An operating voltage and grey level of the display panel 300 of the embodiment is shown in FIG. 6 in which black is shown at both sides and white is shown in the middle. That is, in a case of an operating voltage 10V applied for controlling the rotation of liquid crystal, the display panel 300 will be black if the operating voltage is 10V or 0V. On the contrary, the display panel 300 will be white if the operating voltage is 5V. Positive polarity is in the region between 5V and 10V and negative polarity is in the region between 0V and 5V respectively. Preferably, there are 256 gray scales between black and white. In some other embodiment of the display panel 300, it is possible of arranging white at both sides and black in the middle depending on designs desired by display panel manufacturers.

The operation unit 3212 is adapted to receive display data representing a voltage vector of no polarity in which the larger of the value of display data the closer to 10V or 0V the voltage will be. The operation unit 3212 is also adapted to receive one of a plurality of polarity data vectors in the storage unit 3211 and a corresponding PAC signal (e.g., a first set of polarity

data vector). The element of the polarity data vector is data polarity in which the corresponding element of the vector is +1 when the data polarity is positive and on the contrary, the corresponding element of the vector is -1 when the data polarity is negative (step S501).

5 Next, the operation unit 3212 performs an inner product operation with respect to the polarity data vector and the display data vector for obtaining an absolute value of the inner product as a result. That is, the result corresponds to a sum of coupling voltages of the PAC signals of the polarity data vector. For example, the result is +4 (step S502). The result then is sent
10 to the comparison unit 3213 for comparing with a predetermined value (e.g., +5). It means that the coupling value of the corresponding PAC signal of the polarity data (i.e., the absolute value of the sum of coupling voltages) is smaller if the result is smaller than the predetermined value per the comparison in the comparison unit 3213. As an end, it is possible of
15 decreasing cross-talk and improving display quality. Finally, the comparison unit 3213 outputs the PAC signal to the data driver 330 so that the data driver 330 is able to control the polarity arrangement of liquid crystal of the display panel 300 in response to the PAC signal (step S503).

 The comparison unit 3213 will output an enable signal to the counting
20 unit 3214 for incrementing the counting unit 3214 by one (1) if the result is larger than the predetermined value. Accordingly, the storage unit 3211 is able to sequentially output a second set of polarity data vector and the corresponding PAC signal to the operation unit 3212 (step S504). Next, the operation unit 3212 performs an operation with respect to the new polarity

data vector for obtaining a corresponding sum of coupling voltages (step S502). Next, the corresponding sum of coupling voltages is sent to the comparison unit 3213 for comparing with the predetermined value again. The above loop will end once the sum of coupling voltages of the polarity data vector is smaller than the predetermined value. Subsequently, the comparison unit 3213 sends the corresponding PAC signal of the polarity data vector to the data driver 330 (step S503). The corresponding PAC signal of the polarity data vector having the smallest sum of coupling voltages will be outputted if the sum of coupling voltages of each of all polarity data vectors is larger than the predetermined value.

A flow chart of a second preferred embodiment of the invention is illustrated in FIG. 8 in conjunction with FIG. 7. The block diagram of FIG. 7 is similar to that of FIG. 4 except that the counting unit 3214 is not required. The process of FIG. 8 begins in step S801 in which the operation unit 3212 receives display data vector and the storage unit 3211 stores polarity data vector. The operation unit 3212 then performs an inner product operation with respect to the polarity data vector and the display data vector for obtaining an absolute value of the inner product as a result. The result corresponds to a sum of coupling voltages of each set of polarity data vector (step S802). The result then is sent to the comparison unit 3213 for comparing with each other so as to choose the polarity data vector having a smallest sum of coupling voltages and the corresponding PAC signal. As an end, it is possible of decreasing cross-talk. Finally, the comparison unit 3213 outputs the chosen PAC signal to the data driver 330 (step S803).

In view of the foregoing, it is known that, in the invention, a plurality of sets of polarity data and a plurality of corresponding PAC signals are stored in advance, and then an operation is performed with respect to one set of polarity data and the display data for obtaining a corresponding sum of coupling voltages. The sum of coupling voltages of one set of polarity data is compared with a predetermined value. If the sum of coupling voltages of one set of polarity data is smaller than the predetermined value, the corresponding PAC signal of the polarity data is outputted to the data driver. Alternatively, the sums of coupling voltages of the sets of polarity data are compared with each other so as to choose the polarity data having a smallest sum of coupling voltages and the corresponding PAC signal for output. As an end, it is possible of obtaining an optimum polarity arrangement, decreasing cross-talk, and improving display quality.

Although the present invention has been explained in relation to its preferred embodiment, it is to be understood that many other possible modifications and variations can be made without departing from the spirit and scope of the invention as hereinafter claimed.